

L Number	Hits	Search Text	DB	Time stamp
4	31602	((timings\$2 separation\$2) near9 (circuits\$5 generat\$5 filp-flop\$2)) AND (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop")	USPAT	2004/04/14 09:54
5	1934	342/124,175,205.cc1s. 73/290R, 290V.cc1s.) (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.	USPAT	2004/04/14 09:57
6	201	324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.	USPAT	2004/04/14 09:55
7	34	((timings\$2 separation\$2) near9 (circuits\$5 generat\$5 filp-flop\$2)) AND (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop")) and (342/124,175,205.cc1s. 73/290R, 290V.cc1s.) (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.)	USPAT	2004/04/14 09:57
8	123	342/124.cc1s.	USPAT	2004/04/14 10:59
9	679279	((time\$2 timings\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop")	USPAT	2004/04/14 10:59
10	66197	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop").ab.	USPAT	2004/04/14 10:58
11	787	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop") and (342/124,175,205.cc1s. 73/290R, (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.)	USPAT	2004/04/14 10:59
12	84	((time\$2 timings\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop") and 342/124.cc1s.	USPAT	2004/04/14 10:59
13	142	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop").ab.) and (342/124,175,205.cc1s. 73/290R, 290V.cc1s.) (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.)	USPAT	2004/04/14 10:59
14	20	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop").ab.) and 342/124.cc1s.	USPAT	2004/04/14 10:59
15	82	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop") and (342/124,175,205.cc1s. 73/290R, (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.) and (flip-flops\$1 "D-flipflop" "D-flipflop" "filplop" "d flip flop")	USPAT	2004/04/14 11:14
16	11	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop") and 342/124.cc1s.) and (flip-flops\$1 "D-flipflop" "D-flipflop" "filplop" "d flip flop")	USPAT	2004/04/14 11:01
17	6	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop").ab.) and 342/124.cc1s.) and (flip-flops\$1 "D-flipflop" "D-flipflop" "filplop" "d flip flop")	USPAT	2004/04/14 11:06
18	27	((time\$2 timing\$2 separation\$2) near9 (control\$2 generat\$5 detect\$5 sens\$5 difference\$5 chatter\$5)) (flip-flops\$1 "D-flipflop" "D-flip-flop" "filplop" "d flip flop").ab.) and (342/124,175,205.cc1s. 73/290R, 290V.cc1s.) (324/644.cc1s. 73/304R, 304C, 305-322, 322.5.cc1s.) and (flip-flops\$1 "D-flipflop" "D-flipflop" "filplop" "d flip flop") (transmis\$5 same receiv\$5 same (separat\$5 control\$2 timing\$1 time\$2 chatter\$2))	USPAT	2004/04/14 11:01
19	208377		USPAT	2004/04/14 11:09

-	52	((timings\$2 separation\$2) near9 (circuit\$5 generat\$5 flip-flop\$2))) and (flip-flop\$2)	USPAT	2004/04/14 09:54
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1 Storage optimization by replacing some flip-flops with latches

Tsung-Yi Wu; Youn-Long Lin;

Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sept. 1996

Pages:296 - 301

[Abstract] [PDF Full-Text (636 KB)] IEEE CNF

2 Array of sensors with A/D conversion based on flip-flops

Lian, W.; Wouters, S.E.;

Instrumentation and Measurement, IEEE Transactions on , Volume: 39 , Issue: 4 , Aug. 1990

Pages:653 - 657

[Abstract] [PDF Full-Text (432 KB)] IEEE JNL

3 Maximum operating frequency in Si bipolar master-slave toggle flip-flop circuit

Ishii, K.; Ichino, H.; Yamaguchi, C.;

Solid-State Circuits, IEEE Journal of , Volume: 29 , Issue: 7 , July 1994

Pages:754 - 760

[Abstract] [PDF Full-Text (504 KB)] IEEE JNL

4 Partial scan design based on levelised combinational structure

Park, S.; Lee, G.;

Computers and Digital Techniques, IEE Proceedings- , Volume: 145 , Issue: 4 , July 1998

Pages:249 - 254

[Abstract] [PDF Full-Text (552 KB)] IEE JNL

5 Configuring flip-flops to BIST registers

Stroele, A.P.; Wunderlich, H.-J.;

Test Conference, 1994. Proceedings., International , 2-6 Oct. 1994

Pages:939 - 948

6 Computing optimal clock schedules

Szymanski, T.G.;

Design Automation Conference, 1992. Proceedings., 29th ACM/IEEE , 8-12 June 1992

Pages:399 - 404

7 Linearization of the timing analysis and optimization of level-sensitive digital synchronous circuits

Taskin, B.; Kourtev, I.S.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 12 , Issue: 1 , Jan. 2004

Pages:12 - 27

8 Fast and energy-frugal deterministic test through test vector correlation exploitation

Sinanoglu, O.; Orailoglu, A.;

Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on , 6-8 Nov. 2002

Pages:325 - 333

9 On the use of VHDL simulation and emulation to derive error rates

Lima, F.; Rezgui, S.; Carro, L.; Velazco, R.; Reis, R.;

Radiation and Its Effects on Components and Systems, 2001. 6th European Conference on , 10-14 Sept. 2001

Pages:253 - 260

10 Optimal design of synchronous circuits using software pipelining techniques

Boyer, F.-R.; Aboulhamid, El.M.; Savaria, Y.; Bennour, I.E.;

Computer Design: VLSI in Computers and Processors, 1998. ICCD '98.

Proceedings., International Conference on , 5-7 Oct. 1998

Pages:62 - 67

11 Built-in self testing of sequential circuits using precomputed test sets

Iyengar, V.; Chakrabarty, K.; Murray, B.T.;

VLSI Test Symposium, 1998. Proceedings. 16th IEEE , 26-30 April 1998

Pages:418 - 423

12 Fixed-phase retiming for low power design

Lalgudi, K.N.; Papaefthymiou, M.C.;

Low Power Electronics and Design, 1996., International Symposium on , 12-14 Aug. 1996

Pages:259 - 264

**13 A MODular and Reprogrammable Real-time Processing Hardware,
MORRPH**

Drayer, T.H.; King, W.E., IV.; Tront, J.G.; Conners, R.W.;
FPGAs for Custom Computing Machines, 1995. Proceedings. IEEE Symposium
on , 19-21 April 1995
Pages:11 - 19

[Abstract] [PDF Full-Text (976 KB)] IEEE CNF

**14 Property-based test generation for scan designs and the effects of the
test application scheme and scan selection on the number of detectable
faults**

Pomeranz, I.; Reddy, S.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions
on , Volume: 21 , Issue: 5 , May 2002
Pages:628 - 637

[Abstract] [PDF Full-Text (362 KB)] IEEE JNL

15 Active timing multilevel fault-simulation with switch-level accuracy

Meyer, W.; Camposano, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions
on , Volume: 14 , Issue: 10 , Oct. 1995
Pages:1241 - 1256

[Abstract] [PDF Full-Text (1504 KB)] IEEE JNL

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